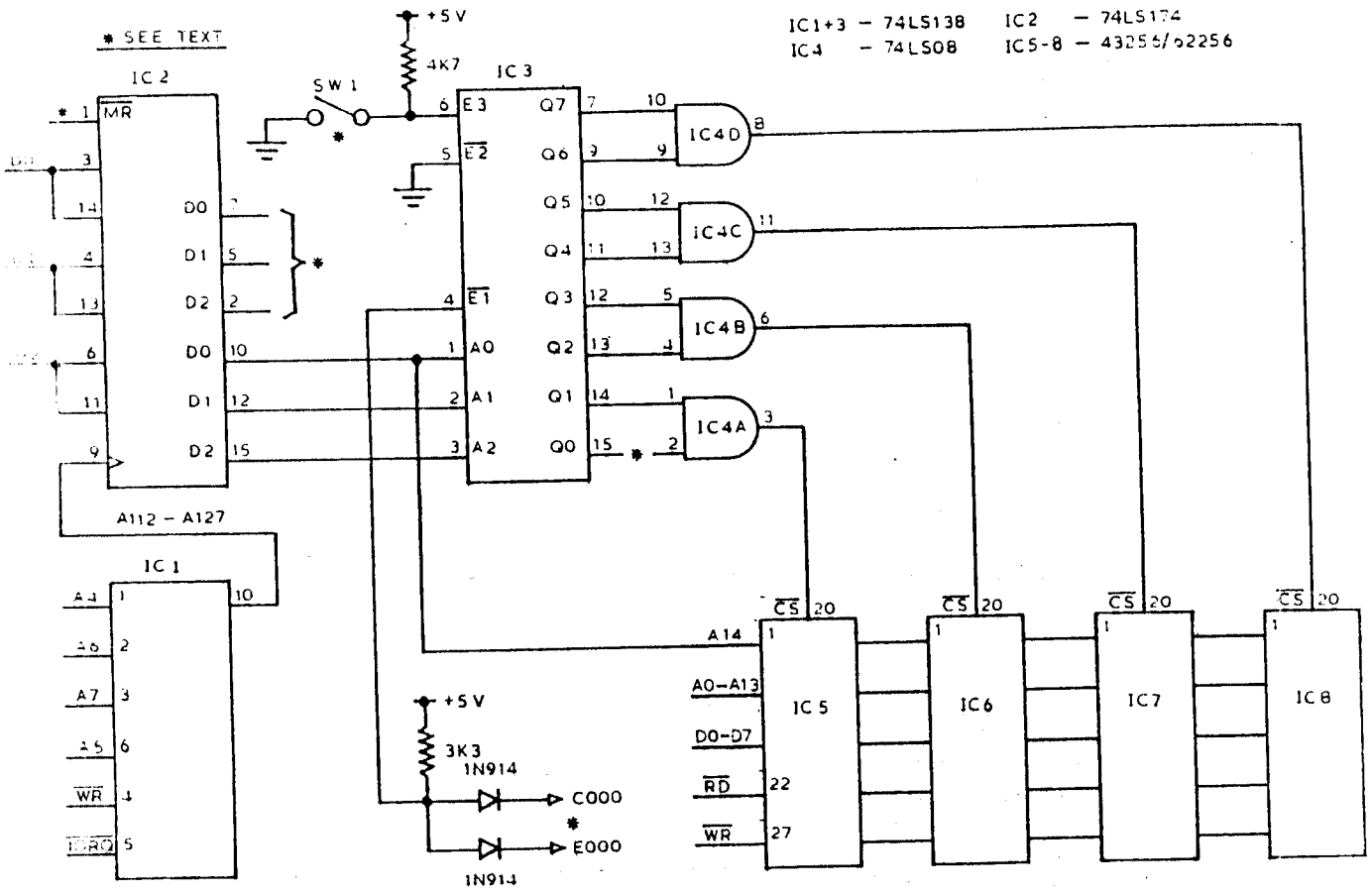
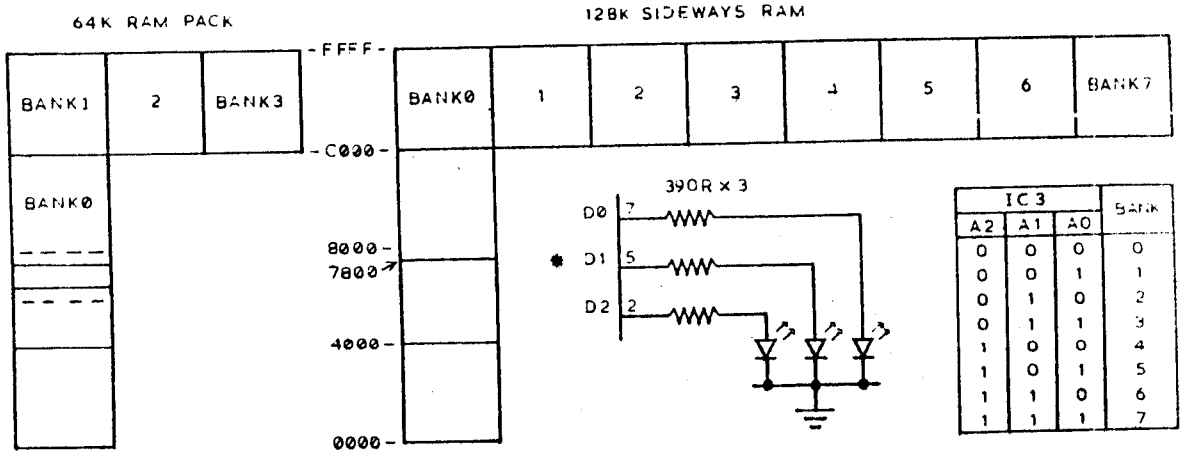
VZ 200/300 128K SIDEWAYS RAM (C) JOSEPH P. LEON 1988





IC 3			BANK
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

NOTE ON IC'S 1 to 4 :-

Although 74LS Series IC'S are shown in above circuit and they will work as designed but if possible get for :-

IC1-74HCT138 IC2-74HCT174 IC3-74HC138 IC4-74HC08

The 74HCT Series are designed to interface between TTL and CMOS IC'S while the 74HC Series can drive TTL or CMOS IC'S. The HC/HCT IC'S have much lower power cosumption than 74LS IC'S, comparable speed and are preferable. The VZ power supply has its limits and every IC added puts an added load on the supply.

VZ 64K memory cartridges are very hard if not impossible to get. For that reason I decided to design my own and this 128K SIDEWAYS RAM project is the result and it will give you more memory than you'll ever use.

Not all of you will need the full 128K and for that reason it was designed to start with 32K and expand in 32K steps as funds allow or need arises. And now to the circuit description. Construction details will be given in next issue.

We'll start with a look at the 64K RAM PACK. Of course as you may have realised by now the VZ memory map does not allow for more than 34K of user RAM, so BANK SWITCHING techniques must be used. The block diagram of 64K Ram Pack says it all. Each of the four banks consists of 16K blocks. Bank 0 is fixed between 32K and 48K while bank 1 resides at 48K to 64K and is the default at power up. Banks 2 and 3 can be switched in when desired.

Now if you have a look at 128K S/Ways Ram block diagram you'll notice that all 8 banks from 0 to 7 reside between 48K and 64K with only one bank available at any one time. By adding the 18K of Ram below 48K we get a total of 146K ram available to the user which puts a few big brand name computers to shame. And now to the circuit proper.

IC 1) The 74LS138 provides a decoded output in the address range of 112 to 127 which is used to trigger the latch.

IC 2) The 74LS174 is a HEX LATCH and was chosen so duplicate outputs could be obtained. One lot of outputs is used to select desired bank while the second lot of outputs are used to drive LEDS to indicate bank selected.

IC 3) This 74LS138 is used to decode banks 0 to 7.

IC 4) The 74LS08 is a quad and gate and each gate is used to enable each 32K Ram twice. The ZERO DATA line which goes to each A14 on the 32K RAMS is used to enable top or bottom 16K block on each 32K Ram chip.

IC 5-8) These chips are 32K X 8 Static Cmos Ram Memory Chips. They come under two different numbers - 43256 or 62256. Both are same exept they are made by different companies.

To understand the operation of this circuit as a whole you have to know or learn a bit about the BINARY system and digital logic. Refer to the truth table for IC 3.

* Pin 1 MR IC2 - This pin is connected to pin 2 (Reset) of edge connector. This has the effect of synchronized RESET of 128K Ram and VZ at power up.

* SW1 - This switch serves two functions.
1) Switch CLOSED - All O/P's on IC 3 are forced High which in turn puts a High on each O/P of IC 4 disabling all 32K Ram IC'S thus allowing WORDPRO cartridge operation.
2) Switch CLOSED before power up then OPENED after power up. This has the effect of lowering DOS communication region and T.O.M. below 48K and very usefull with disk drives.

* D0, D1 & D2 IC2 - These O/P's are used to drive LEDS to indicate selected bank and are optional.

* C000 & E000 - These I/P's require decoded 8K blocks in the range C000-FFFF and are used to enable the 32K Ram chips via IC3 & IC4. More on them in next issue.

* Q0 Pin 15 IC3 - As it stands the 128K S/Ways Ram is not compatible with existing 64K programs using bank switching because bank 0 is at 48K to 64K. The circuit changes (Minor) will be given next issue to make it compatible with the 64K Ram Pack.